WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device, comprising:

a plurality of non-volatile memory cells each of which has a storage structure and an electrically alterable parameter representing data of at least two bits, wherein the electrically alterable parameters of the plurality of non-volatile memory cells are shiftable to at least three mutually different first, second and third program states from an erase state;

reference value generating circuitry generating first, second and third programming reference values for programming the first, second and third program states, and generating first, second and third read reference values, which are different from the first, second and third programming reference values, for reading the first, second and third program states; and

sensing/program-verifying circuitry receiving the parameter of one non-volatile memory cell, the first, second and third read reference values and the first, s cond and third read programming reference values;

wherein the first read referenc value is allocated between the first program state and the second program state, the second read reference value is allocated between the second program state and the third program state, and the third read reference value is allocated between the third program state and the erase state,

wherein the second read reference value is allocated substantially at a midpoint between the second program state and the third program state, and the first read reference parameter is shifted toward the second program state from a midpoint between the first program state and the second program state,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the electrically alterable parameter, verifies whether the electrically alterable parameter is shifted to the parameter indicating a selected one state of the first, second and third program states, and programs the electrically alterable parameter until it has been verified that the electrically alterable parameter has been shifted to the selected one state,

wherein the first, second and third programming reference values are used for verifying whether the

electrically alterable parameter is shifted to the first, second or third program state, and the first, second and third read reference values are used for detecting whether the electrically alterable parameter is near to the first, second or third program state, and

wherein the reference value generating circuitry generates the first, second and third programming reference values and the first, second and third read reference values such that one of the first, second and third programming reference values and the first, second and third read reference values is shifted from and dependent upon the other.

2. A non-volatile semiconductor memory device according to claim 1,

wherein a shift amount of one of the first, second and third read reference values from the corresponding one of the first, second and third programming reference values is dependent upon the corresponding one of the first, second and third programming reference value.

3. A non-volatile semiconductor memory device according to claim 1,

wherein the reference value generating circuitry includes:

a first reference value generating circuit which generates the first programming reference value and the first read reference value,

a second reference value generating circuit which generates the second programming reference value and the second read reference value, and

a third reference value generating circuit which generates the third programming reference value and the third read reference value, and

wherein each of the first reference value generating circuit, the second reference value generating circuit and the third reference value generating circuit includes an element causing the corresponding read reference value and the corresponding programming reference value to have different values.

4. A non-volatile semiconductor memory device according to claim 3,

wherein each of the first reference value generating circuit, the second reference value generating circuit and the third reference value generating circuit further includes a reference cell which has substantially the same

construction as each of said plurality of memory cells, and the reference cell and the element of each reference value generating circuit cooperate to provide a predetermined difference between the corresponding read and programming reference values.

5. A non-volatile semiconductor memory device according to claim 1,

wherein each read reference value is dependent upon the corresponding programming reference value.

6. A non-volatile semiconductor memory device according to claim 1,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the state indicating the erase state, the first program state, the second program state and the third program state, and

wherein the programming states of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the erase state by an erase operation.

7. A non-volatile semiconductor memory device according to claim 6,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by hot electron injection.

8. A non-volatile semiconductor memory device according to claim 6,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by Fowler-Nordheim tunneling.

9. A non-volatile semiconductor memory device according to claim 2,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the state indicating the erase state, the first program state, the second program state and the third program state, and

wherein the programming states of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the erase state by an erase operation.

10. A non-volatile semiconductor memory device according to claim 9,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by hot electron injection.

11. A non-volatile semiconductor memory device according to claim 9,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by Fowler-Nordheim tunneling.

12. A non-volatile semiconductor memory device according to claim 3,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the state indicating the erase state, the first program state, the second program state and the third program state, and

wherein conductivity values of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the erase state by an erase operation.

13. A non-volatile semiconductor memory device according to claim 12,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by hot electron injection.

14. A non-volatile semiconductor memory device according to claim 12,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by Fowler-Nordheim tunneling.

15. A non-volatile semiconductor memory device according to claim 4,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the state indicating the erase state, the first program state, the second program state and the third program state, and

wherein conductivity values of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the erase state by an erase operation.

16. A non-volatile semiconductor memory device according to claim 15,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by hot electron injection.

17. A non-volatile semiconductor memory device according to claim 15,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by Fowler-Nordheim tunneling.

18. A non-volatile semiconductor memory device according to claim 5,

wherein a conductivity value of the one non-volatile memory cell is decreased in order of the state indicating the erase state, the first program state, the second program state and the third program state, and

wherein conductivity values of non-volatile memory cells of one of a byte, a block and a chip level can be shifted to the erase state by an erase operation.

19. A non-volatile semiconductor memory device according to claim 18,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by hot electron injection.

20. A non-volatile semiconductor memory device according to claim 18,

wherein each of the plurality of non-volatile memory cells has a floating gate to which electrons are capable of being injected from a channel by Fowler-Nordheim tunneling.

21. A non-volatile semiconductor memory device according to claim 1,

wherein the first, second and third read reference values are dependent upon the first, second and third programming reference values, respectively.